Original Article

A Low Power 6T SRAM using SleepPower Reduction Technique

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Abstract: *One type of memory component is static random access memory (SRAM). SRAM is in high demand in SOCs due to its unique data-retention capabilities. For the sake of anticipating future needs, this memory part became the subject of study. The importance of power leakage in chip design has grown as SRAM densities have increased. Recent years have seen significant progress in SRAM's ability to reduce power consumption. Mary methods have been developed to provide both dynamic and static power reduction. Today's memory technology is primarily concerned with improving speed and reducing power consumption. In light of this, the research focuses on a low power SRAM that employs a hybrid sleep transistor approach and compares it to traditional SRAM in terms of delay: power dissipation and power delay product(PDP). Using this method, the delay and power requirements of SRAM are decreased. All parameters and stimulations are based on the TANNER MENTORGRAPHICS 250nm technology.*

Keywords: *SRAM, System on chip (Soc), MTCMOS,Scaling.*

I. INTRODUCTION

Demand for high-speed, portable gadgets like notebooks, computers, PDAs, mobile phones, etc., that run on batteries has been on the rise recently. These gadgets necessitate a quicker primary memory. Refreshment isn't always required. The biggest challenge with high-speed SRAM is power consumption. It has a devastating effect on the battery life of mobile devices. Power-efficient SRAM architecture is hence recommended. Supply voltage scaling keeps power consumption under control, yet supply voltage scaling has its limits due to high performance requirements. Therefore, it may not be necessary to rely solely on supply voltage scaling to keep power consumption within the bounds mandated by power-sensitive applications. In addition to scaling the supply voltage, low power designs need circuit and system level approaches.[1].

According to the data in the accompanying graph, power loss increases as technology is reduced in size.[2] Multimedia apps on mobile devices can either be actively used or placed in a standby state. A mobile device, for instance, has a low activity factor if its idle time is disproportionately greater than its active time. In a perfect world, various optimization strategies have been devised to counteract this loss. The leakage current in a CMOS transistor comes from four different places [10].
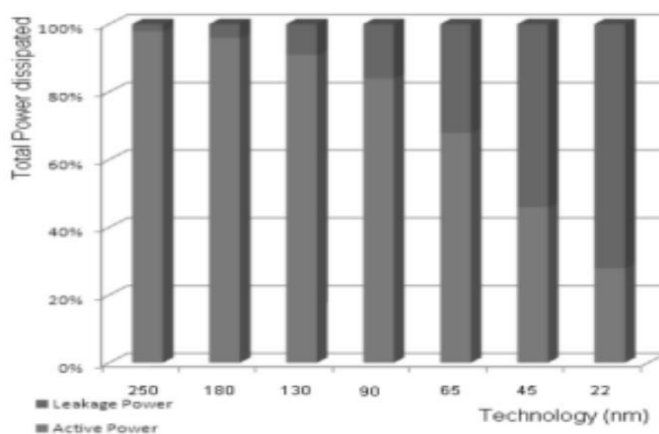

Figure 1: Power Dissipation in Various Technologies

The low threshold voltage causes the sub threshold leakage current, the ultra-thin oxide causes the gate leakage

current, and the extensively doped profile causes the tunneling leakage current. Raising the threshold voltage is one strategy for doing so. Now, gate-to-source and gate-to-drain overlap currents, direct tunneling current (also called gate-to-channel current and gate-to-substrate current), and leakage current all have significant effects on tunneling current [7].

The goal of this research is to create a memory cell that consumes minimal energy. To lessen power consumption, this work proposes a novel approach based on a sleep transistor for SRAM cells, and experimental findings demonstrate the impact of voltage scaling for lónm CMOS technology now on the market. The remaining sections of the paper are structured as follows. Read/write/hold operations and the typical SRAM architecture are discussed in Section II. In Section III, we compare and contrast the proposed qualities with those of existing logic styles. Simulation findings are presented in Section IV. In the final section, we draw some conclusions.

II. CONVENTIONAL 6T SRAM CELL

The traditional 6T memory cell, depicted in the following picture, consists of four NMOS transistors and two PMOS transistors, all of which are cross-coupled with two pass transistors that are connected to a set of complementary bit lines. Leakage currents of both CMOS inverters will be modest, limiting the memory cell's leakage power consumption. When compared to resistive load and depletion-load NMOS SRAM Cell [6], the sole drawback of using cross-coupled inverters is a slightly larger size. The states of an SRAM cell are

- Write
- Read
- Hold

A. Hold State:

The circuit will be at rest and the word line will be deactivated when in hold mode. Bitline-connecting transistors Ml and M have been disabled. The cell is inaccessible during the hold state. As long as the supply voltage is maintained, the cross-coupled inverters will continue to feed back into each other. In the hold mode, the latch will be used to save the information.

B. Read State:

The first step of a read operation is to fully charge Bit and Bit bar. The memory cells M3 and M6 are activated. The MI and M are activated when the word line is affirmed. Q and Q' are converted to bit-Line values. Since M does not conduct electricity, Bit bar is set to "1" (M and M6 raise it to VW) and Bit line discharges through MI and M3.
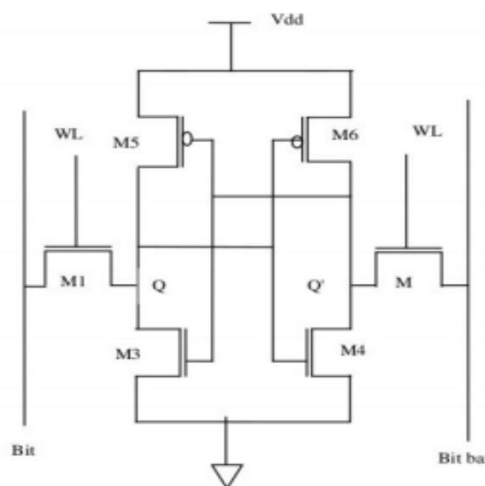

Figure 2: Read State Diagram

C. Write State:

At first, the bitline pairs (BLB and BL) are subjected to a forced differential voltage (VDD and 0). The information to be written at the O and O' storage nodes is represented by a differential voltage that is under the control of the write drivers. After that, the WL is enabled to commit the data from the bit-line pairs to their respective storage nodes. Let's pretend that Q and Q' initially hold the values l' and '0'. An access transistor (MI) linked to BL (at '0') is activated whenever the WL is asserted. Through M3 and Ml, voltage and current travel from VDD to BL. The potential at node 0 is reduced due to this

current flow. For a write operation to succeed, the ratio of the pull-up transistor (M3) to the access transistor (MI) must be less than the trip point of the inverter (M6 & M4). The pull-up to ratio describes this relationship.

According to the description of the 6T SRAM cell's operation given above, there are two distinct sources of power dissipation in SRAM. The first is the dynamic power required for data read/written, transistor switching, and bit/bit-bar line charging/discharging [3]. The second is during steady-state operation of the cells due to MOS transistor leakage current.
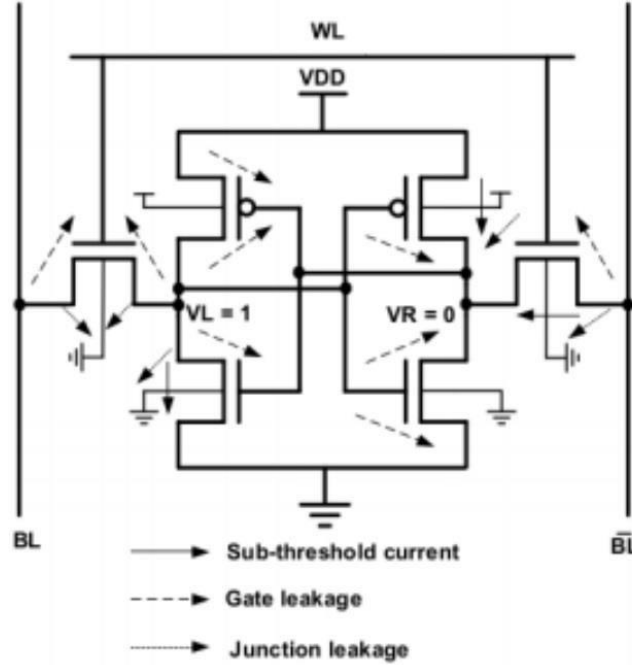

Figure 3: Leakage Currents in 6T SRAM

III. SLEEP TRANSISTOR TECHNIQUE

The sleep transistor design methodology is one of the low power design methods for 6T SRAM, with the lowest power dissipation [9]. The dual sleep transistor arrangement is used in this method. The cell is coupled in series with one Pmos and one Nmos transistor. Pmos is connected between Vd and pull-up transistors. The pull-down transistors are linked with Nmos. To simulate ground and virtual V, these sleep transistors are used. When the circuit is active, the sleep transistor is turned on to keep everything running normally, but when it is off, the source node of the gate floats and the leaking path is severed. Reduced power consumption is mostly attributable to two factors: transistor stacking and low sub-threshold leakage current in high V devices.
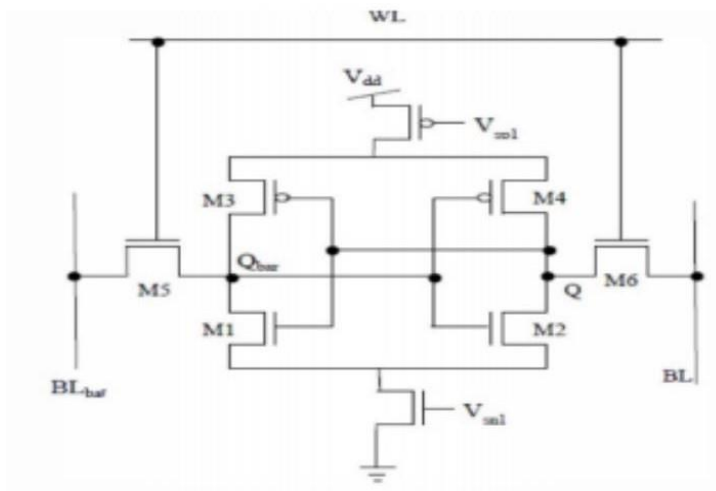

Figure 4: SRAM using Sleep Transistor Technique

IV. MODIFIED DESIGN

Adopting MTCMOS technology allowed for more well-rounded cell stability, performance, and write margin. Supply voltage and device choice also impact SRAM's power consumption [4]. MTCMOS and its hybrid counterpart, Hybrid MTCMOS, are functionally equivalent. Specifically, this makes use of a stacked PMOS sleep transistor with a low threshold voltage. In the suggested layout, the NMOS sleep transistor is activated while the PMOS sleep transistor is disabled. The power dissipation is cut in half when using both negative and positive voltage [5].
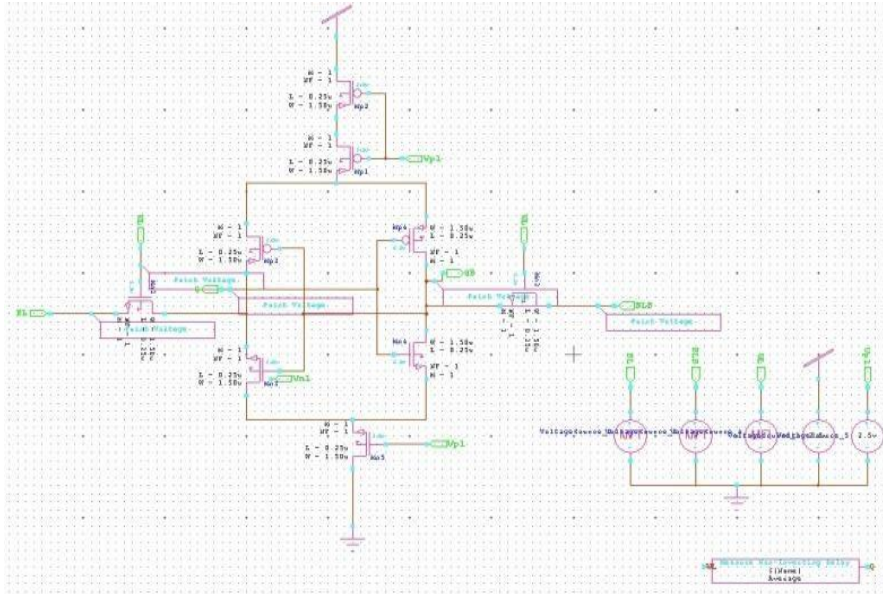

Figure 5: Modified Design

In this case, transistor size is the most critical factor. The read stability and write capability of an SRAM cell are both directly affected by the transistor size [6]. If you want your circuit to be stable, make sure the width of your pull-down transistors is much larger than that of your access or pull-up transistors [8]. In this configuration, sleep transistors should have the same width as pull-down transistors. Figure 3 shows that the diameter of PMOS sleeps transistors needs to be half that of NMOS sleep transistors. In this case, both PMOS and NMOS sleep transistors share a common Vpl.

V. SIMULATION & RESULTS

Conventional 6T SRAM and the proposed SRAM have been compared with regards to power consumption and latency. The TANNER Mentor Graphics tool is used for all simulations in this work, and the technology used is 250nm. For the suggested design, the wave form at the output looks like in the figure.
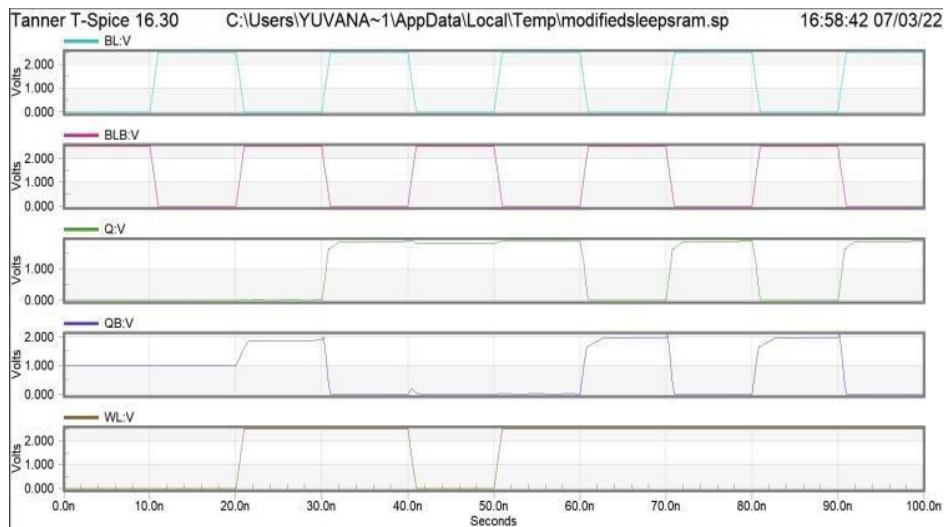

Figure 6: Simulation Waveform of Modified Design

Table 1: Average Power Consumption and Delay Report of Different SRAMs

Vdd=Vgs=2.5v	Avg power consumption	Delay (in Ns)
SRAM 6T CONVENTIONAL	1.958×10^{-4}	15.1319
SRAM FORCED STACK	1.27×10^{-5}	15.0851
SRAM SLEEP	7.598×10^{-8}	15.0344
DTMOS SRAM 6T	2.287×10^{-4}	15.1413
DTMOS FORCED STACK	1.085×10^{-5}	15.0303
DTMOS SLEEP	2.7157×10^{-11}	15.1505
VTMOS SRAM 6T	8.65×10^{-5}	19.2338
VTMOS FORCED STACK	6.7131×10^{-6}	14.7376
VTMOS SRAM SLEEP	4.563×10^{-13}	15.0822
MODIFIED SLEEEP	4.875×10^{-8}	15.0345

VI. CONCLUSION

In order to reduce the amount of power consumed by SRAM, we have implemented a hybrid and VTMOS sleep approach in this research. Power consumption, power dissipation, and power delay product are all dramatically decreased by our approach. It has been determined that the proposed design uses 60% less power than standard SRAM while having 2% less latency. Automatic Memory Recall While Sleeping Compared to other SRAMs, (VTMOS, DTMOS, MODIFIED) uses less energy.

VII. ACKNOWLEDGMENT

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